UM10061

ISP1302 eval board

Rev. 01 — 3 April 2007 **User manual**

Document information

Info	Content
Keywords	usb; universal serial bus; isp1302
Abstract	This document explains the ISP1302 eval board.

Revision history

Rev	Date	Description
01	20070403	First release.

Contact information

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1. Introduction

The ISP1302 is a Universal Serial Bus (USB) On-The-Go (OTG) transceiver device that is fully compliant with *Universal Serial Bus Specification Rev. 2.0* and *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.0a.* It integrates a USB full-speed and low-speed transceiver, and other analog components to fully support the OTG functionality.

The ISP1302 is ideal for use in portable electronics devices, such as mobile phones, Personal Digital Assistants (PDAs), digital still cameras and digital audio players. The ISP1302 acts as a physical layer to interface with any USB OTG Controller.

The ISP1302 evaluation (eval) board is designed to evaluate the functions of the ISP1302 chip. The main components on the board are: the ISP1302 (in HVQFN24 or WCSP25 package), I^2C-bus master, USB mini-AB connector, analog audio interface and USB OTG Controller interface. Operation mode of the ISP1302 can be configured through the I^2C-bus interface. The OTG status and control registers in the ISP1302 can also be accessed through the I^2C-bus interface.

To verify the functions of the ISP1302 by using the DOS test program that is provided with the eval kit, connect the ISP1302 eval board to the parallel port of a PC. To fully verify the functions of the ISP1302, a USB OTG Controller is used to connect to the ISP1302 board through the defined interface connector.

Fig 1 shows the ISP1302 eval board.

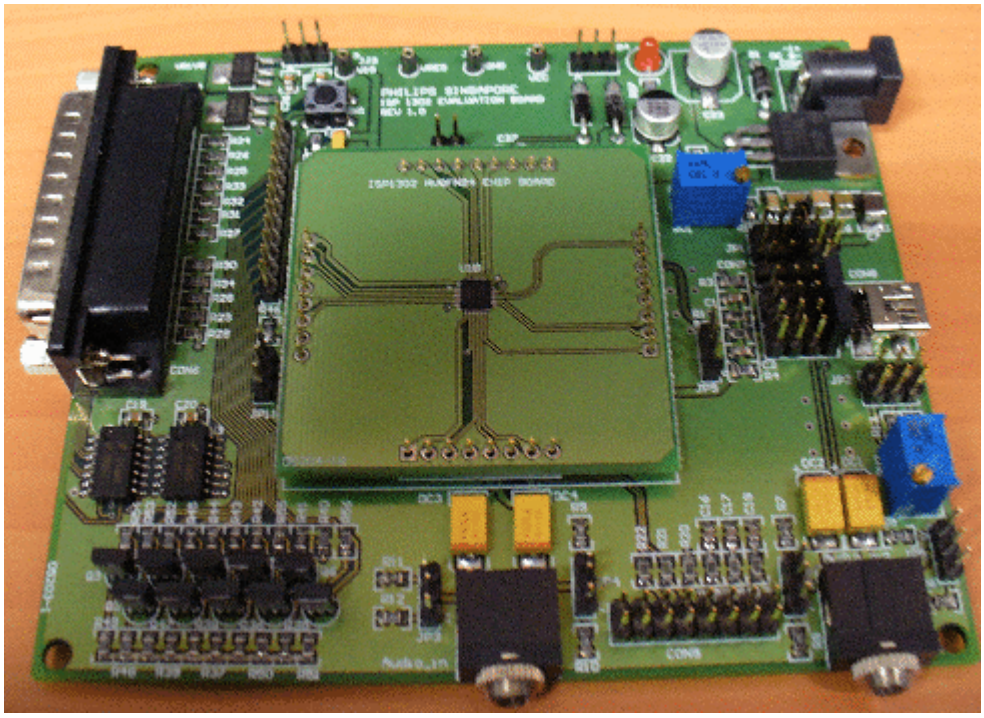

Fig 1. ISP1302 eval board PCB layout

2. System requirements

An x86 PC with a DB-25 parallel port is required. The test program runs on DOS (or the command line in Microsoft Windows 98). The test program is compiled using Turbo C++ Ver. 3.0.

3. Configurations and settings

3.1 Power requirements

By default, the ISP1302 board is powered by an 8 V-to-15 V power supply through the DC jack (CON10). The V_{CC} power can also be supplied from the USB mini-AB connector (CON8). When the V_{CC} power is correctly applied to the board, LED D4 (red) will be turned on.

Table 1. V_{CC} power selection

Jumper	Description
JP12	**Short 1 and 2**: V_{CC} from the USB mini-AB connector (CON8) **Short 2 and 3**: V_{CC} from the DC jack (CON10)

Similarly, the power supply for the $V_{CC(I/O)}$ pin of the ISP1302 can be provided either from the onboard +3.3 V source or from the onboard 1.8 V source.

Table 2. $V_{CC(I/O)}$ selection

Jumper	Description
JP5	**Short 1 and 2**: $V_{CC(I/O)}$ from the onboard +1.8 V source **Open 2 and 3**: $V_{CC(I/O)}$ from the onboard +3.3 V source

3.2 Carkit DP interrupt detector setting

The carkit interrupt detector can be enabled or disabled by a jumper.

Table 3. Carkit interrupt detector setting

Jumper	Description
JP9	**Short 1 and 2**: Enable the carkit interrupt detector **Short 2 and 3**: Disable the carkit interrupt detector

3.3 DP and DM connection setting

Table 4. DP and DM connection setting

Jumper	Description
JP6, JP7	**Short 1 and 2**: Connect DP and DM to mini-AB connectors **Short 2 and 3**: Connect DP and DM to AUDIO OUT connectors **Short 5 and 6**: Connect DP and DM to the UART connector (CON9) **Short 7 and 8**: Pull DP and DM to HIGH through a 1.5 kΩ resistor

3.4 USB interface

There is a USB mini-AB connector on the ISP1302 eval board.

- If an OTG controller is connected to the ISP1302, the USB port functions as an OTG dual-role device.
- If a Host Controller is connected to the ISP1302, the USB mini-AB port functions as a host.
- If a Peripheral Controller is connected to the ISP1302, the USB mini-AB port functions as a device.

3.5 Audio interface

The ISP1302 eval board has an interface to support an analog audio carkit application. Connect:

- The audio carkit to the AUDIO OUT socket or the mini-AB connector on the board.
- The audio input line signal to the AUDIO IN socket on the board.

3.6 Reset

For a hardware reset to the ISP1302, press the manual reset switch (SW1). The reset pulse (active LOW) can also come from the I^2C-bus interface (pin 7 of CON6 and pin 10 of CON7).

4. Test program 1302.exe

4.1 Introduction

DOS test program 1302.exe is provided to help you verify the functions of the ISP1302 chip. The program uses the PC parallel port to access the ISP1302 registers through the I^2C-bus interface. The program simulates the software I^2C-bus master at the Hardware Abstraction Layer (HAL).

The test program can do the following:

- Set the I^2C-bus slave address for the ISP1302.
- Reset all registers to their default values.
- Display the current value of all registers on your PC screen.
- Write any value to a writable register.
- Set the mode of operation of the ISP1302, such as, USB function and suspend mode, transparent I^2C-bus mode, transparent general-purpose buffer mode, and global power-down mode.
- Enable or disable the charge pump of the ISP1302.

4.2 Launching the application program

If your PC boots to pure DOS, run the test program on the command line. If your PC boots to Microsoft Windows 98, open an MS-DOS window and run the test program. It is recommended that you boot the PC to pure DOS.

To run the test program, type **1302**[1] and press the **Enter** key at the A:> prompt.

1. In this document, items that you type, click or press are indicated in **bold**.

4.3 Using menus

After the program is launched, the main menu will appear on the screen. See Fig 2.

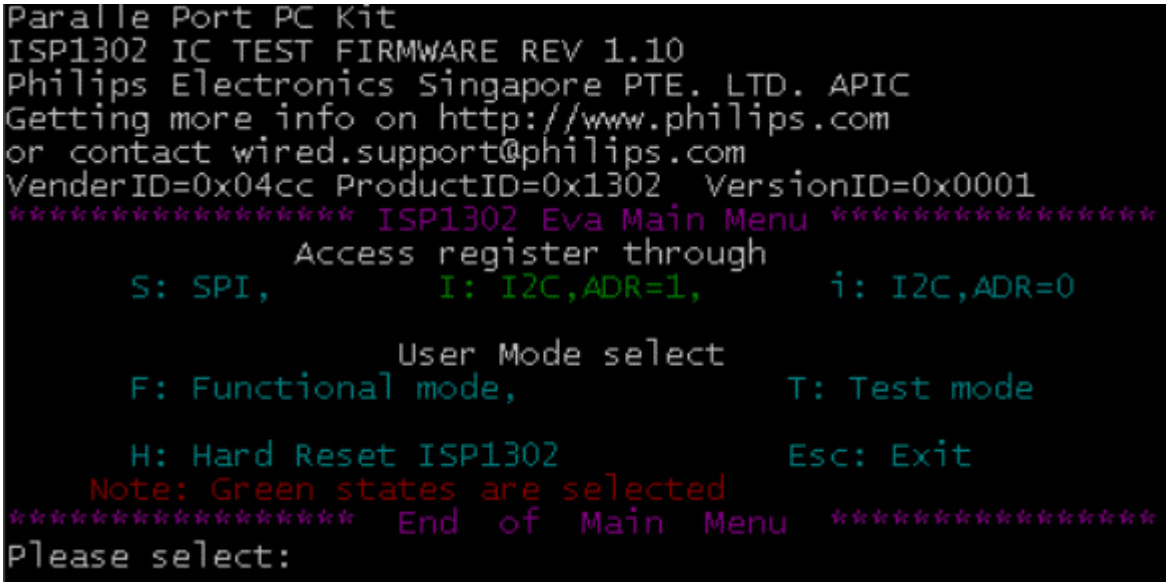

Fig 2. Test program main menu

In the main menu screen, selecting any item S, I, i, F, T or H will perform the desired action. To exit the program, press **Esc**.

The following subsections describe menu items.

4.3.1 Choosing the I²C-bus slave address for the ISP1302

- If the **I** key is pressed, ADR will be HIGH. The slave address for the ISP1302 will become 5Ah.
- If the **i** key is pressed, ADR will be LOW. The slave address for the ISP1302 will become 58h.
- If the **S** key is pressed, the I²C-bus host will work in SPI host mode (not available for the ISP1302).

Ensure that choices are correctly done; otherwise, other operations may fail.

4.3.2 Hard resetting the ISP1302

On pressing key **H**, the program will issue a hardware reset to the ISP1302.

4.3.3 Choosing user mode

- On pressing the **F** key, a submenu will appear on the screen. See Fig 3. The program will work in functional mode.
- When the **T** key is pressed, a submenu will appear on the screen. See Fig 4. The program will work in test mode.

4.3.4 Functional mode submenu

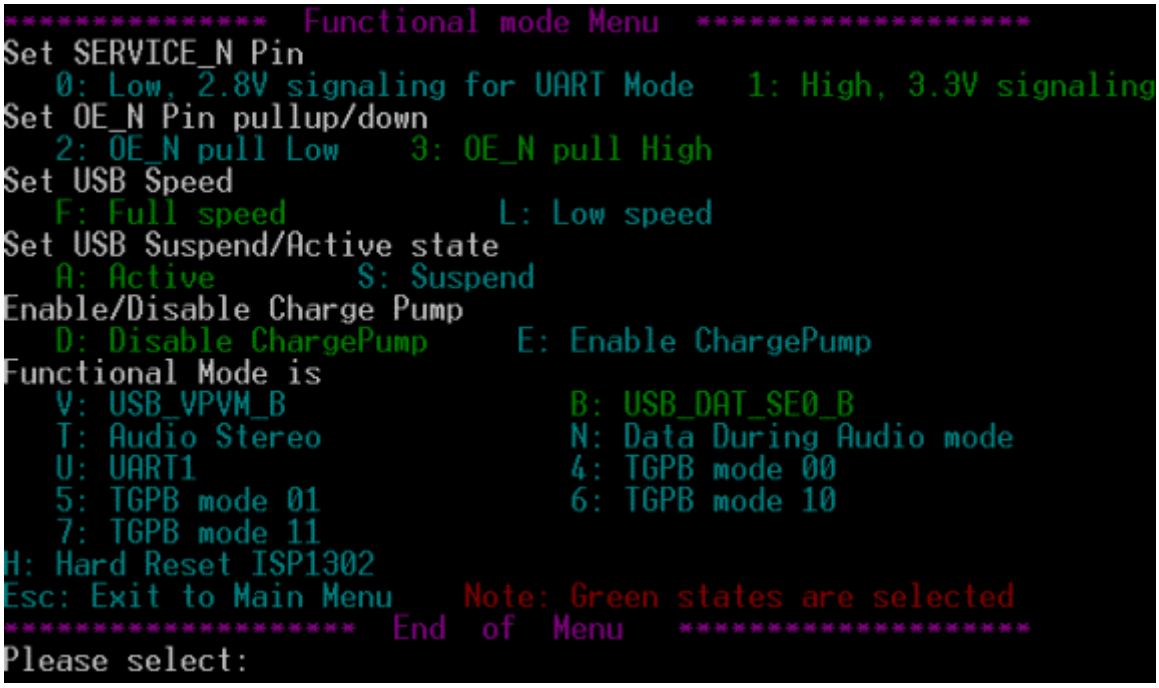

Fig 3. Functional mode submenu

4.3.4.1 SERVICE_N pin setting

- If key **0** is pressed, the SERVICE_N pin will be pulled to LOW.
- If key **1** is pressed, the SERVICE_N pin will be pulled to HIGH.

4.3.4.2 OE_N pin setting

- If key **2** is pressed, the OE_N pin will be pulled to LOW.
- If key **3** is pressed, the OE_N pin will be pulled to HIGH.

4.3.4.3 USB speed setting

- If key **F** is pressed, the USB transceiver will work in full-speed mode.
- If key **L** is pressed, the USB transceiver will work in low-speed mode.

4.3.4.4 USB suspend and active setting

- If key **S** is pressed, the USB transceiver will be in USB suspend mode.
- If key **A** is pressed, the USB transceiver will be in USB normal mode.

4.3.4.5 Enabling or disabling the charge pump

- Pressing key **E** will enable the charge pump.
- Pressing key **D** will disable it.

4.3.4.6 Functional mode setting

- On pressing key **V**, the ISP1302 will be in USB VP_VM mode.
- On pressing key **B**, the ISP1302 will be in USB DAT_SE0 mode.

- On pressing key **T**, the ISP1302 will be in transparent audio mode.
- On pressing key **N**, the ISP1302 will be in data-during-audio mode.
- On pressing key **U**, the ISP1302 will be in transparent UART mode.
- On pressing key **4**, the ISP1302 will be in transparent general-purpose buffer mode. TRANSP_BDIR[1:0] = 00.
- On pressing key **5**, the ISP1302 will be in transparent general-purpose buffer mode. TRANSP_BDIR[1:0] = 01.
- On pressing key **6**, the ISP1302 will be in transparent general-purpose buffer mode. TRANSP_BDIR[1:0] = 10.
- On pressing key **7**, the ISP1302 will be in transparent general-purpose buffer mode. TRANSP_BDIR[1:0] = 11.

4.3.4.7 Hard resetting the ISP1302

- On pressing key **H**, the program will issue a hardware reset to the ISP1302.

4.3.5 Test mode submenu

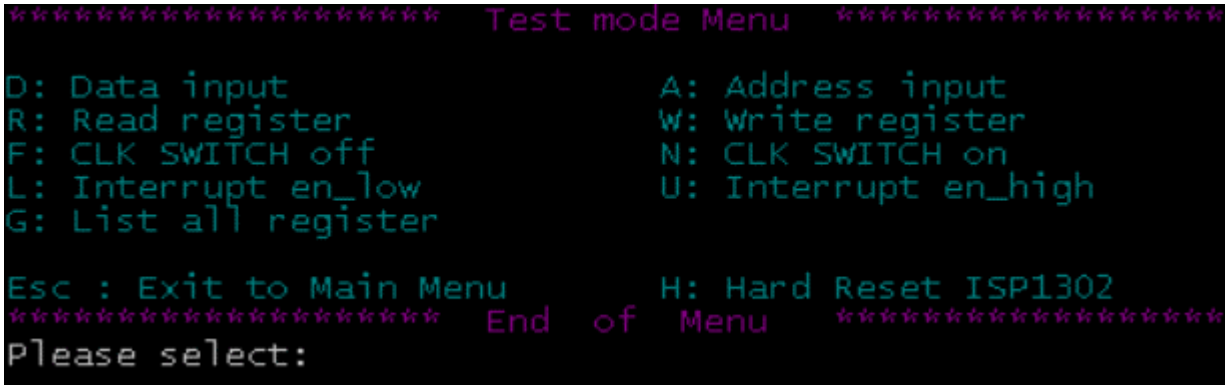

Fig 4. Test mode submenu

4.3.5.1 Data or address input

- On pressing key **D**, you can input an 8-bit data and save it in the data buffer of the program.
- On pressing key **A**, you can input an 8-bit data and save it in the address buffer of the program.

4.3.5.2 Read or write register

- On pressing key **R**, the program will read the register address and display the value of this register on the screen.
- On pressing key **W**, the program will write data to the register address.

4.3.5.3 Clock setting

- If key **F** is pressed, the program will turn off the internal clock of the ISP1302 and set it in power-down mode.
- If key **N** is pressed, the program will turn on the internal clock.

4.3.5.4 Interrupt setting

- On pressing key **L**, the program will enable all low interrupts and disable all high interrupts.
- On pressing key **U**, the program will enable all high interrupts and disable all low interrupts.

4.3.5.5 Listing all registers

- On pressing key **G**, the program will display all the registers on the screen.

4.3.5.6 Hard resetting of the ISP1302

- On pressing key **H**, the program will issue a hardware reset to the ISP1302.

5. Hardware description

5.1 Block diagram

Fig 5 shows the block diagram of the ISP1302 eval board.

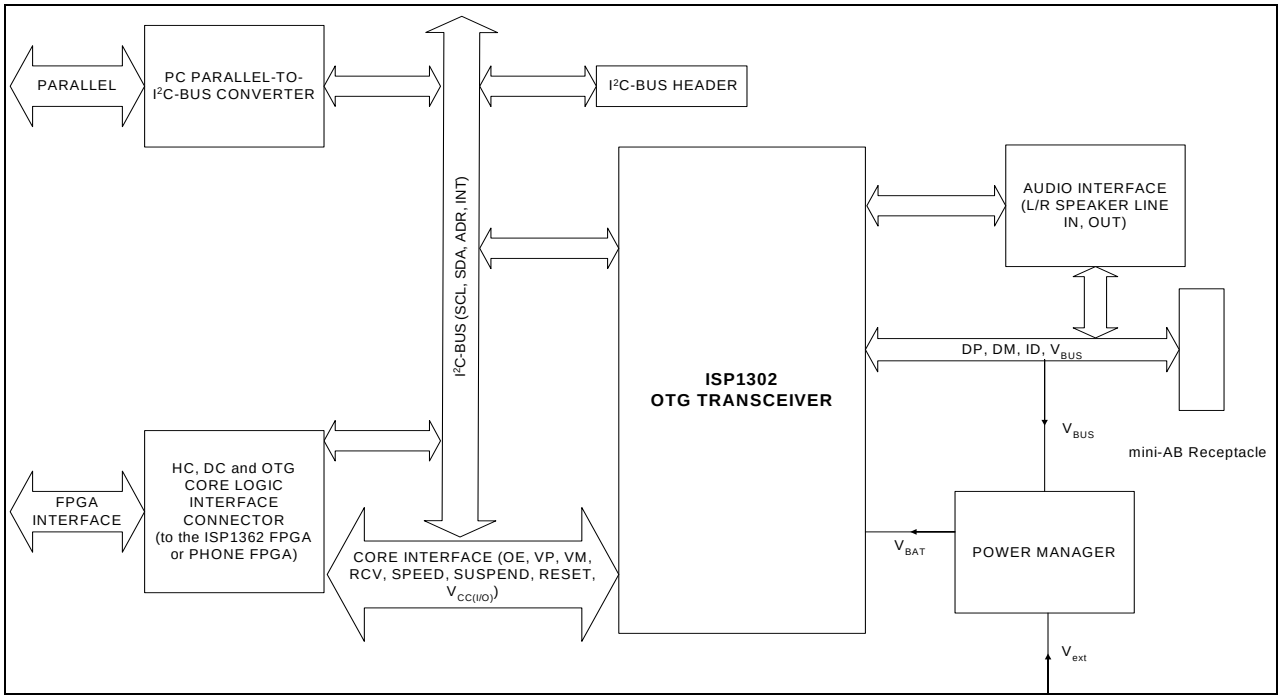

Fig 5. Block diagram of the ISP1302 eval board

5.2 Functional description

A brief description of each function module is given in following subsections.

5.2.1 I²C-bus header

This block connects the ISP1302 I²C-bus to the external I²C-bus Host Controller.

5.2.2 PC parallel to the I²C-bus converter

This interface provides an alternative method to access the ISP1302 I²C-bus interface through the PC. The PC must emulate the software I²C-bus master to access the ISP1302 I²C-bus slave.

5.2.3 Host Controller, Peripheral Controller and OTG core logic interface connector

This interface provides connection to a Host Controller, Peripheral Controller or OTG core logic. This interface is used during the OTG system-level evaluation or compliance testing.

5.2.4 Power manager

This block includes the “8 V-to-15 V” to 5 V, 5 V-to-3.3 V and 5 V-to-1.8 V regulator and power source selection.

5.2.5 Audio interface

This block provides stereo audio line IN interface and stereo audio line OUT interface. Its main purpose is to demonstrate the carkit application, that is, play audio or voice with carkit.

6. Connector pin information

6.1 CON6 pin assignment

CON6 is used to connect to the PC parallel port through the DB-25 printer cable. For pin assignments, see Table 5.

Table 5. CON6 pin assignments

Pin no.	Signal	Direction IN/OUT
1	nStrobe	P_SDAOUT
2	Data0	P_CS_ADR
3	Data1	P_SCL
4	Data2	P_SEL
5	Data3	P_SUSPEND
6	Data4	P_SERVICE_N
7	Data5	P_RESET
8	Data6	n.c.
9	Data7	P_OE_N
10	nAck	P_MISO
11	Busy	P_INT
12	Paper-Out/Paper-End	P_SDAIN
13	Select	SELECT_IN

Pin no.	Signal	Direction IN/OUT
14	nAuto-Linefeed	n.c.
15	nError/nFault	n.c.
16	nInitialize	n.c.
17	nSelect-Printer/ nSelect-In	n.c.
18 to 30	Ground	n.c.
21 to 25	Ground	GND

6.2 CON7 pin assignment

CON7 is a 12 x 1 header interface used to connect to an I^2C-bus Host Controller. Table 6 shows CON7 pin assignment.

Table 6. CON7 pin assignment[1]

Pin no.	Pin name
1	$V_{CC(I/O)}$
2	GND
3	ADR
4	SCL
5	SDA
6	MISO
7	SEL
8	SUSPEND
9	SERVICE
10	RESET
11	OE
12	INT

[1] n. c.—Denotes no connection.

6.3 CON5 pin assignment

CON5 is an 8 x 2 interface header used to connect the ISP1302 to the USB OTG Controller core. CON5 includes USB Serial Interface Engine (SIE) signals DAT_VP, SE0_VM, RCV, OE_TP_INT_N and GND. The pin assignment for CON5 is given in Table 7.

Table 7. CON5 pin assignment

Pin no.	Pin name	Pin no.	Pin name
1	OE_N	9	VP

Pin no.	Pin name	Pin no.	Pin name
2	GND	10	GND
3	DAT_VP	11	VM
4	GND	12	GND
5	SE0_VM	13	n.c.
6	GND	14	GND
7	RCV	15	n.c.
8	GND	16	GND

7. Schematics of the eval board

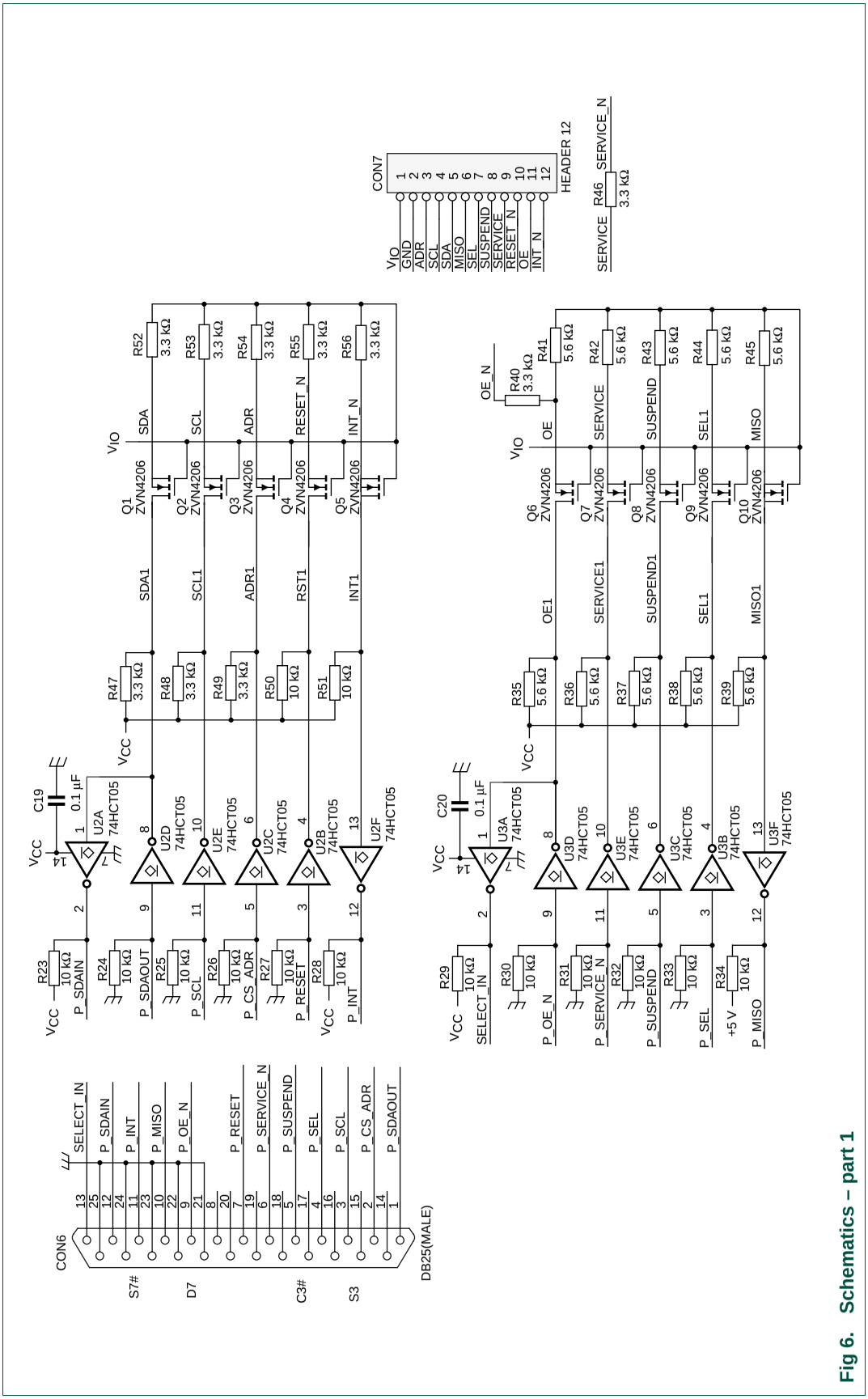

Fig 6. Schematics – part 1

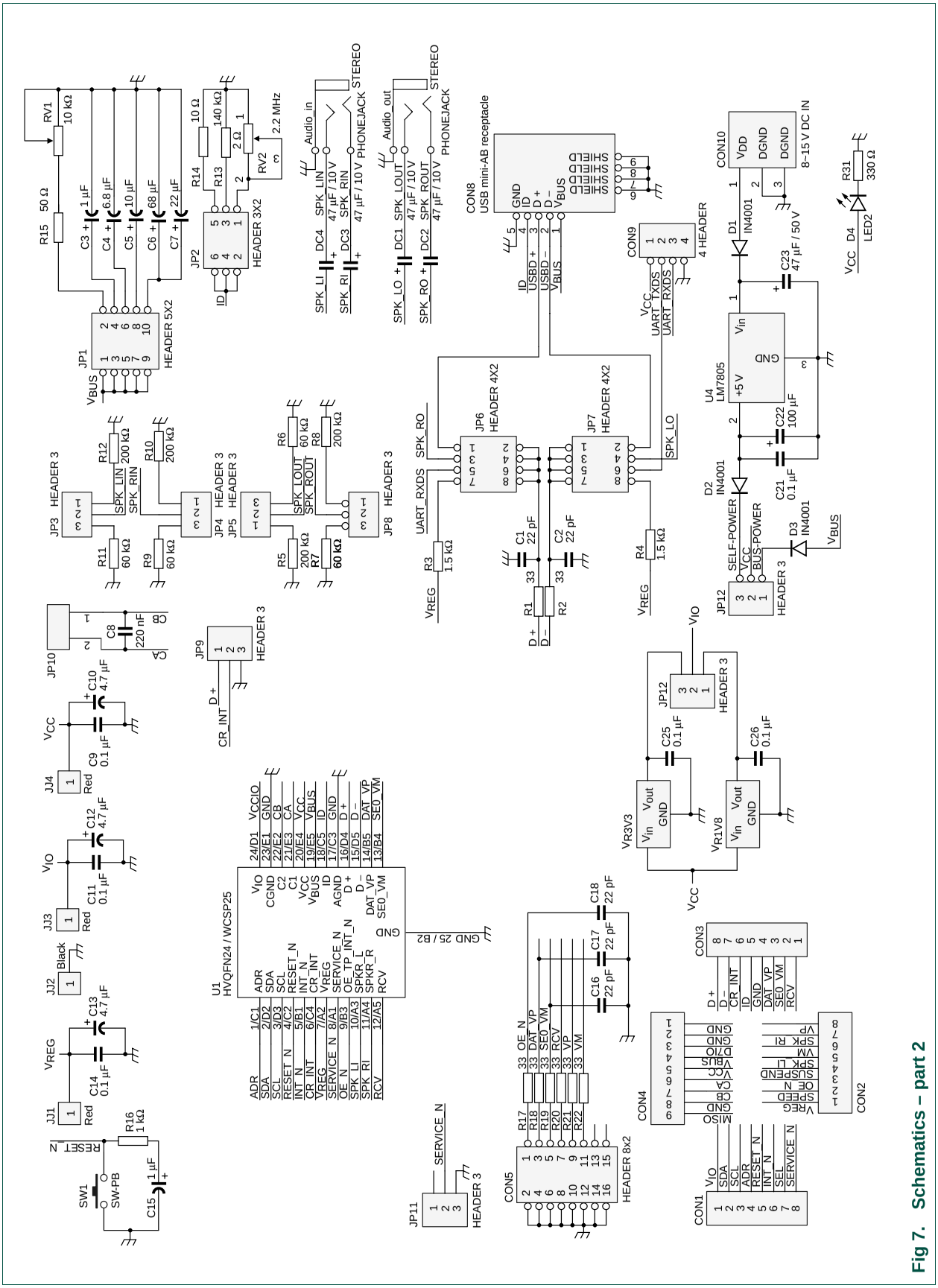

Fig 7. Schematics – part 2

8. Bill of materials

Table 8. BOM of the ISP1302 eval board

Designator	Description	Footprint	Comments
CON1 CON2 CON3	Header, 8-pin	HDR1 X 8	-
CON4	Header, 9-pin	HDR1 X 8	-
JP10	Jumper	HEADER 2	-
VR1V8 VR3V3	Voltage regulator	SIP-G3/Y2	-
C21	Capacitor	-	0.1 µF
C9 C11 C14 C19 C20 C25 C26	Capacitor	0805	0.1 µF
R3 R4	Resistor	0805	1.5 kΩ
R14	Resistor	0805	10 Ω
C22	Electrolytic capacitor	-	100 µF
R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R50 R51 R55 R56	Resistor	0805	10 kΩ
RV1	Potentiometer	VAR R	10 kΩ
C5	Capacitor	CASE B	10 µF
R13	Resistor	0805	140 kΩ
R16	Resistor	0805	1 kΩ
C3 C15	Capacitor	CASE A	1 µF
RV2	Potentiometer	VAR R	2.2 MΩ
R5 R8 R10 R12	Resistor	0805	200 Ω
C8	Capacitor	0805	220 nF
C1 C2 C16 C17 C18	Capacitor	0805	22 pF
C7	Capacitor	CASE C	22 µF
R40 R46 R47 R48 R49 R52 R53 R54	Resistor	0805	3.3 kΩ
R1 R2 R17 R18 R19 R20 R21 R22	Resistor	0805	33 Ω
CON9	4-pin header	-	4 header
C10 C12 C13	Capacitor	CASE B	4.7 µF
C23	Electrolytic capacitor	-	47 µF / 50 V
DC1 DC2 DC3 DC4	Electrolytic capacitor	Case D	47 µF 10 V
R35 R36 R37 R38 R39 R41 R42 R43 R44 R45	Resistor	0805	5.6 kΩ

Designator	Description	Footprint	Comments
R15	Resistor	0805	50 Ω
C4	Capacitor	Case B	6.8 µF
R6 R7 R9 R11	Resistor	0805	60 kΩ
C6	Capacitor	Case D	68 µF
U2 U3	Hex inverter (open-drain)	SOP-14	74HCT05
CON10	Connector	DC-JACK	8~15 V DC IN
JJ2	Test point	B JACK	Black
CON6	Connector	DB-25/M	DB25 (male)
CON7	12-pin header	-	Header 12
JP3 JP4 JP5 JP8 JP9 JP11 JP12	Jumper	-	Header 3
JP2	Jumper	Header 3 X 2	Header 3 x 2
JP6 JP7	Jumper	-	Header 4 x 2
JP1	Jumper	Header 5 X 2	Header 5 x 2
CON5	Header	Header 8 X 2	Header 8 x 2
U1	OTG transceiver	HVQFN24	HVQFN24 / WCSP25
D1 D2 D3	Diode	IN4001	IN4001
D4	LED	LED	LED2
U4	Voltage regulator	TO-3	LM7805
AUDIO_IN AUDIO_OUT	Audio connector	-	Phone jack stereo
JJ1 JJ3 JJ4	Test point	B JACK	Red
SW1	Button	TACT-SW	SW-PB
CON8	Connector	USB mini-AB	USB mini-AB receptacle
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10	Transistors	TO92	ZVN4206

9. Abbreviations

Table 9. Abbreviations

Acronym	Description
HAL	Hardware Abstraction Layer
OTG	On-The-Go
PCB	Printed-Circuit Board
SIE	Serial Interface Engine

Acronym	Description
USB	Universal Serial Bus

10. References

- ISP1302 Universal Serial Bus On-The-Go transceiver with carkit support data sheet
- Universal Serial Bus Specification Rev. 2.0
- On-The-Go Supplement to the USB 2.0 Specification Rev. 1.0a
- ISP1302 errata

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12. Contents

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